REMARKS

The applicants have carefully considered the Office action dated May 21, 2004 and the references it cites. By way of this Response, claims 1, 4, 7-10, 13, 17-19, 22-24, 26-28 and 31-32 have been amended. In view of the following, it is respectfully submitted that all pending claims are in condition for allowance and favorable reconsideration is respectfully requested.

As an initial matter, the applicants note that claims 14-16 stand allowed and are not discussed in the following.

As a further initial matter, the applicants note that the Office action objected to allowable claims 8, 9, 26 and 27 for being dependent on rejected base claims. In response, the applicants have rewritten claims 8, 9, 26 and 27 in independent form. (Claims 8 and 9 have both been broadened by deleting the phrase "a first time" from the first element of the claims). Accordingly, as acknowledged in the Office action, claims 8, 9, 26 and 27 are allowable. Claims 8, 9, 26 and 27 will not be discussed further herein.

As requested in the Office action, claim 19 has been amended to provide proper antecedent basis for the term "main memory." Thus, the objections to claims 19-23 have been overcome.

By way of this response, the specification has been amended to correct minor typographical errors and to make this application a continuation-in-part of U.S. patent application serial number 10/057,493, now U.S. Patent 6,775,748. A substitute declaration including the priority claim will be filed shortly. No new matter has been added.

Before addressing the art rejections, the applicants note that signed copies of the PTO-1449 forms were not returned with the Office action. The

Office is requested to provide the same with the next communication in this application. A further information disclosure statement is being filed with this response citing Intel's US. Patent 6,775,748 and the references cited in that Patent.

Turning to the art rejections, the Office action rejected claims 1-7, 10-13, 17-25 and 28-32 as being unpatentable over one or more of Chang, U.S. Patent 6,519,685 (assigned to Intel) and O'Leary, U.S. Patent 5,867,162. The applicants respectfully traverse these rejections.

Claim 1 is patentable over the art cited in the Office action. Claim 1 recites a method of cache intervention comprising providing a copy of a memory block to a third cache from an arbitration winner cache selected based on a predetermined arbitration heierarchy. Although Chang discloses a cache coherency protocol, Chang does not disclose a predetermined arbitration hierarchy to determine which of at least two caches will intervene to provide shared memory block to a third cache.

On the contrary, in the cache coherency protocol defined by Chang, if two caches store an unmodified copy of the same memory block, then only one cache will be in a "Shared-Respond" state, whereas the other cache will be in a "Shared" state. Furthermore, under the Chang protocol, only the cache in the "Shared-Respond" state may provide a copy of the memory block to another cache performing a read request (see Col. 7, Lines 4-13). Moreover, the Shared-Respond" cache is not selected in accordance with a predefined arbitration heierarchy, but instead, the Shared-Respond cache is selected in real time based on a performance criterion. (See Col. 9, lines 33-39 stating "the first caching agent ... to issue a read bus cycle changes its cache line state

from Shared-Temp to Shared-Respond.") Therefore, the cache coherency protocol of Chang does not teach or suggest selecting a cache to provide a shared memory block based on a predefined arbitration hierarchy. On the contrary, it teaches selecting a cache in real time based on a performance criterion (e.g., being first to issue a read bus cycle). Accordingly, Chang does not teach or suggest the combination recited in claim 1.

A brief review of O'Leary reveals that it has nothing to do with cache arbitration. Accordingly, O'Leary cannot overcome the deficiencies of Chang with respect to claim 1. As a result, claim 1 and all claims depending therefrom must be allowed.

Claim 10 is also allowable. Claim 10 recites a multi-processing computing device comprising an arbitration circuit enforcing a fixed cache intervention priority between a first processing agent, a second processing agent and a third processing agent. As discussed above, Chang has a fluid arbitration process, not a fixed arbitration priority between its caches. As such, whether viewed alone or in combination with O'Leary, Chang does not teach or suggest the structure recited in claim 10. Thus, claim 10 and all claims depending therefrom are allowable.

Independent claim 17 is also allowable. Claim 17 recites a computer wherein a first microprocessor or a second microprocessor provides a copy of a memory block to a cache of a third microprocessor based on a predetermined arbitration hierarchy. As discussed above, Chang does not teach or suggest a predetermined arbitration hierarchy. Accodingly, whether viewed alone or in combination with O'Leary, Chang does not teach or suggest the structure of

claim 17. Therefore, claim 17 and all claims depending therefrom must be allowed.

Independent claim 24 is also allowable. Claim 24 recites a method comprising selecting a first cache or a second cache to provide a copy of a memory block to a third cache based on a predetermined hierarcy. As discussed above, neither Chang, O'Leary, nor the combination of Chang and O'Leary, teach or suggest such a method. Accordingly, claim 24 and all claims depending therefrom must be allowed.

Independent claim 28 is also allowable. Claim 28 recites a method of cache intervention comprising preventing a third cache from supplying a copy of a memory block to a second cache if a first cache has a higher cache intervention priority under a predetermined hierarchy. As discussed above, neither Chang, O'Leary, nor the combination of Chang and O'Leary, teach or suggest such a method. Accordingly, claim 28 and all claims depending therefrom must be allowed.

Before closing, the applicants note that the amendments made throughout the claims are either broadening or clarifying and, thus, not necessary for patentability, with the exception of the following amendments:

a) the addition of the "copying the memory block ... with the second cache" clause to claim 1;

b) specifiying that the read request of claim 1 is associated with a third cache and hits the first and second caches;

c) the addition of the "if the memory ...based on a predetermined arbitration hierarchy" clause to claim 1;

d) the amendments to claims 10, 17, and 24; and

e) the addition of the terminal clause to claim 28.

All other amendments not mentioned in the above list (a)-(e) were not necessary for patentability in that they are either broadening or are merely clarifying in that either (a) the amended claims are intended to state the same thing as the claim prior to amendment (i.e., to have the same scope both before and after the amendments) in a more easily understood or more conventional fashion, or (b) the amended claims are dependent on an allowable claim so that any refinement of the dependent claim was not required for patentability, but was made to clarify the claim. Consequently, the amendments not included in the above list (a)-(e) do not give rise to prosecution history estoppel or limit the scope of equivalents of the claims under the doctrine of equivalents.

If the Examiner is of the opinion that a telephone conference would expedite the prosecution of this case, the Examiner is invited to contact the undersigned at the number identified below.

Respectfully submitted,

GROSSMAN & FLIGHT, LLC.
Suite 4220
20 North Wacker Drive
Chicago, Illinois 60606
(312) 580-1020

By: _____
James A. Flight
Registration No. 37,622

Attorneys for Intel Corporation

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